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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,078	08/30/2001	Todd R. Abbott	MIO 0083 PA	7688

7590

09/16/2005

Killworth, Gottman, Hagan & Schaeff, L.L.P.
Suite 500
One Dayton Center
Dayton, OH 45402-2023

EXAMINER

NGUYEN, TUAN H

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	09/943,078		ABBOTT, TODD R.	
	Examiner		Art Unit	
	Tuan H. Nguyen		2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 50-58 is/are pending in the application.
- 4a) Of the above claim(s) 53 and 54 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 58 is/are allowed.
- 6) ☒ Claim(s) 50-52 and 55-57 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 50-52 are rejected under 35 U.S.C. 102(e) as being anticipated by Choi.

See Choi, figs. 1-3 and related text on col. 2-4 which discloses the claimed method for fabricating a semiconductor device including the steps of forming a damascene trench in a first dielectric layer 40 over a base substrate 24, the damascene trench having a gate area 32 in transistor 22C and a local interconnect area 42 (fig. 2); filling the damascene trench with conductive material 44 and planarizing the device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by the conductive material 44 within the damascene trench (see transistor 22C with gate structure 32, 44, and local interconnection structure 42 in fig. 2) wherein the damascene local interconnect structure 42 forms a direct connection to the base substrate 24 through a plug area (see fig. 2, local interconnect structure 42 with conductive material 44 directly connects to the plug area, i.e. the doped region adjacent to S/D region 34 in the substrate 24); shaping

spacers 36 against the vertical walls of the damascene gate structure and the damascene interconnect structure (fig. 2); forming doped S/D regions in the base 24 adjacent and lateral to the damascene gate structure 32, 44 and the damascene local interconnect structure 42.

With respect to claims 51, 52, fig. 2 shows the isolation trench 26 is formed before the first dielectric layer 40, and at least portion of the damascene trench in region 42 partially overlies the isolation trench 26.

Claims 50-52, 55-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al..

See Huang et al., figs. 7-15 and text on col. 3-5 which discloses the claimed method for fabricating a semiconductor device comprising forming a damascene trench in a first dielectric layer 14, 44 over a base substrate, the damascene trench having a gate area and a local interconnect area (fig. 11); depositing a conductive layer 50 over the base substrate such that the damascene trench is filled with a conductive material (fig. 12); planarizing the device to define a damascene structure including a damascene gate 40 and damascene local interconnect structure 43 electrically coupled by the conductive material 50, and the damascene interconnect structure 43 forms a direct connection to region 48 in the base structure (fig. 13); shaping spacers against the vertical walls of the damascene gate structure and the damascene interconnect structure; and forming doped source/drain regions 58 in the base substrate 10 adjacent and lateral to the damascene gate structure 40 and the damascene local interconnect structure 43 (fig. 14).

With respect to claims 51-52, fig. 11 shows isolation trench 12 is formed first in the substrate, and at least a portion of the damascene trench partially overlies the isolation trench 12.

With respect to claim 55, col. 4, next to last paragraph discloses that layer 50 of tungsten or tungsten silicide is deposited over the polysilicon layer.

With respect to claim 56, col. 4, last paragraph discloses the formation of lightly doped drain regions is formed after removing the first dielectric layer 44.

Allowable Subject Matter

Claim 58 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: None of the references of record teaches or suggests the claimed method for forming a semiconductor device including the steps of forming a second patterned mask over the semiconductor device to expose at least a portion of the oxide layer within the local interconnect area for a subsequence of etching and implanting within a plug area.

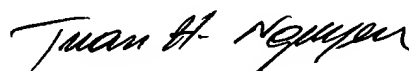
Response to Arguments

Applicant's arguments with respect to claims 50-52, 55-57 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.



Tuan H. Nguyen
Primary Examiner
Art Unit 2813